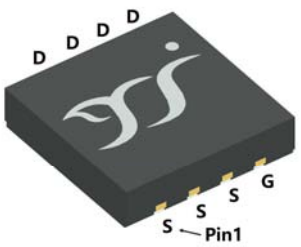
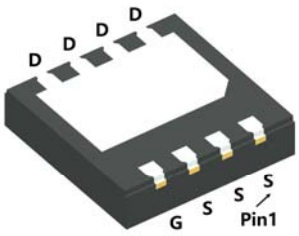
# N-Channel Enhancement Mode Field Effect Transistor

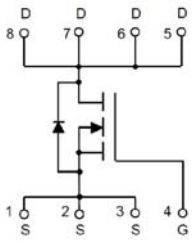



Top View




Bottom View

DFN3333-8L-WF




## Product Summary

- $V_{DS}$ 40V
- $I_D$ 130A
- $R_{DS(ON)}$( at $V_{GS}$=10V) ＜3.5mΩ
- 100% EAS Tested
- 100% ▽$V_{DS}$ Tested

## General Description

- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free
- Part no. with suffix “Q” means AEC-Q101 qualified

## Applications

- Power switching application
- Uninterruptible power supply
- DC-DC convertor
- 12V Automotive systems

## ■ Limiting Values

| Parameter | Conditions | | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|---|
| Drain-source Voltage | | | $V_{DS}$ | - | 40 | V |
| Gate-source Voltage | | | $V_{GS}$ | -20 | 20 | |
| Continuous Drain Current (Note 1,2) | Steady-State | $T_A$=25℃,$V_{GS}$=10V | $I_D$ | - | 20 | A |
| | | $T_A$=100℃,$V_{GS}$=10V | | - | 14 | |
| Continuous Drain Current (Note 1,3) | Steady-State | $T_C$=25℃,$V_{GS}$=10V,Chip limitation | | - | 130 | |
| | | $T_C$=100℃,$V_{GS}$=10V | | - | 92 | |
| Pulsed Drain Current | $T_C$=25℃,$t_p$≤10μs | | $I_{DM}$ | - | 520 | |
| Maximum Body-Diode Continuous Current | $T_C$=25℃ | | $I_S$ | | 80 | |
| Avalanche energy (non-repetitive ) | $T_J$=25℃,$V_G$=10V, $R_G$=25Ω, L=1mH, IAS=18.6A | | EAS | - | 172.98 | mJ |
| Total Power Dissipation (Note 1,2) | Steady-State | $T_A$=25℃ | $P_D$ | - | 2.5 | W |
| | | $T_A$=100℃ | | - | 1.25 | |
| Total Power Dissipation (Note 1,3) | Steady-State | $T_C$=25℃ | | - | 100 | |
| | | $T_C$=100℃ | | - | 50 | |
| Junction and Storage Temperature Range | | | $T_J$ ,$T_{STG}$ | -55 | 175 | ℃ |

## ■Thermal Resistance

| Parameter | | Symbol | Typ | Max | Units |
|---|---|---|---|---|---|
| Thermal Resistance Junction-to-Ambient (Note 2) | Steady-State | $R_{\theta JA}$ | - | 60 | ℃/W |
| Thermal Resistance Junction-to-Case | Steady-State | $R_{\theta JC}$ | - | 1.5 | |

## ■ Ordering Information (Example)

| PREFERED P/N | PACKING CODE | Marking | MINIMUM PACKAGE(pcs) | INNER BOX QUANTITY(pcs) | OUTER CARTON QUANTITY(pcs) | DELIVERY MODE |
|---|---|---|---|---|---|---|
| YJQ3D5G04HQ | F1 | Q3D5G04H | 5000 | 10000 | 100000 | 13“ reel |

## ■ Electrical Characteristics

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Static Parameter** | | | | | | |
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | $V_{GS}$=0V,$I_D$=250μA,Tj=25℃ | 40 | - | - | V |
| | | $V_{GS}$=0V,$I_D$=1mA,Tj=25℃ | 40 | - | - | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$=32V,$V_{GS}$=0V,Tj=25℃ | - | - | 1 | μA |
| | | $V_{DS}$=32V,$V_{GS}$=0V,Tj=125℃ | - | - | 100 | |
| Gate-Source Leakage Current | $I_{GSS}$ | $V_{GS}$=±20V,$V_{DS}$=0V,Tj=25℃ | - | - | ±100 | nA |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$=$V_{GS}$,$I_D$=250μA,Tj=25℃ | 2.2 | 2.8 | 3.7 | V |
| Static Drain-Source On-Resistance | $R_{DS(ON)}$ | $V_{GS}$=10V,$I_D$=20A,Tj=25℃ | - | 2.8 | 3.5 | mΩ |
| Diode Forward Voltage | $V_{SD}$ | $I_S$=20A,$V_{GS}$=0V,Tj=25℃ | - | 0.81 | 1.2 | V |
| Gate Resistance | $R_G$ | f=1MHz,Tj=25℃ | - | 2 | - | Ω |
| **Dynamic Parameters** | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{DS}$=20V,$V_{GS}$=0V,f=1MHz,Tj=25℃ | - | 2134 | - | pF |
| Output Capacitance | $C_{oss}$ | | - | 1093 | - | |
| Reverse Transfer Capacitance | $C_{rss}$ | | - | 76 | - | |
| **Switching Parameters** | | | | | | |
| Total Gate Charge | $Q_g$ | $V_{GS}$=10V,$V_{DS}$=20V,$I_D$=20A,Tj=25℃ | - | 38.2 | - | nC |
| Gate-Source Charge | $Q_{gs}$ | | - | 10.6 | - | |
| Gate-Drain Charge | $Q_{gd}$ | | - | 10.6 | - | |
| Reverse Recovery Charge | $Q_{rr}$ | $I_F$=20A,di/dt=100A/μs,$V_{GS}$=0V,$V_R$=20V, Tj=25℃ | - | 25 | - | nC |
| Reverse Recovery Time | $t_{rr}$ | | - | 31.5 | - | ns |
| Turn-on Delay Time | $t_{D(on)}$ | $V_{GS}$=10V,$V_{DS}$=20V,$I_D$=20A,$R_{GEN}$=3Ω, Tj=25℃ | - | 17 | - | ns |
| Turn-on Rise Time | $t_r$ | | - | 59 | - | |
| Turn-off Delay Time | $t_{D(off)}$ | | - | 28 | - | |
| Turn-off Fall Time | $t_f$ | | - | 16 | - | |

Note：

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. The value of $R_{\theta JA}$ is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 $in^2$ pad of 2oz. Copper, in the still air environment with $T_A$=25℃.The maximum allowed junction temperature of 175℃. The value in any given application depends on the user's specific board design.
3. Thermal resistance from junction to soldering point (on the exposed drain pad).

## ■Typical Electrical and Thermal Characteristics Diagrams

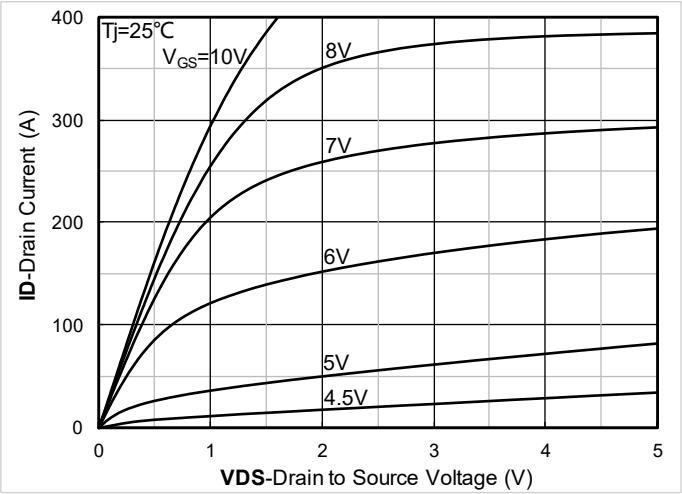



Figure 1. Output Characteristics; typical values

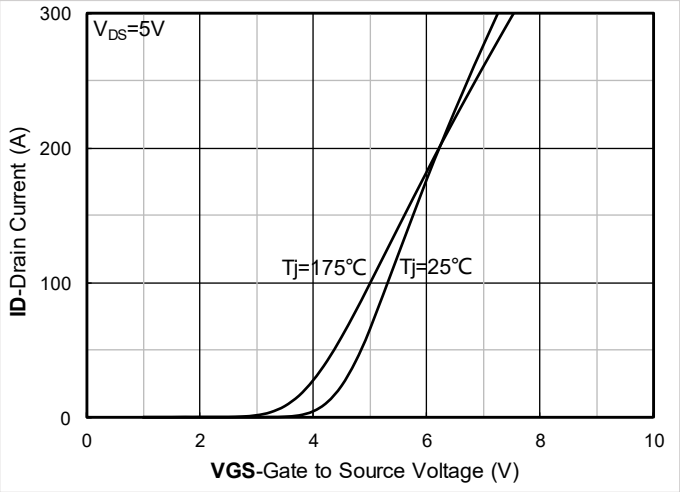



Figure 2. Transfer Characteristics; typical values

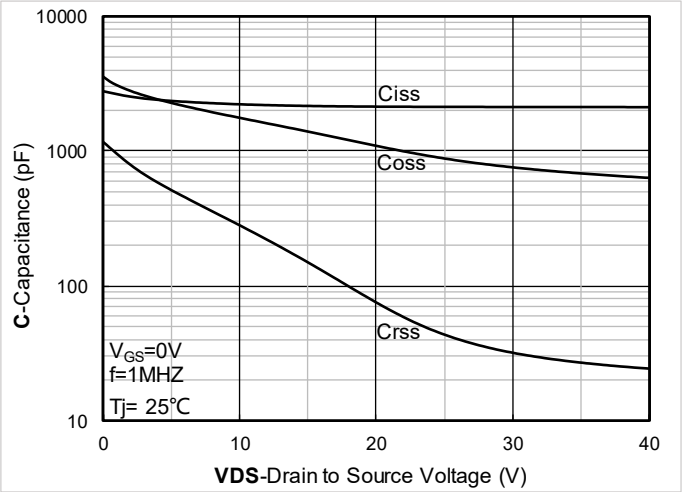



Figure 3. Capacitance Characteristics; typical values

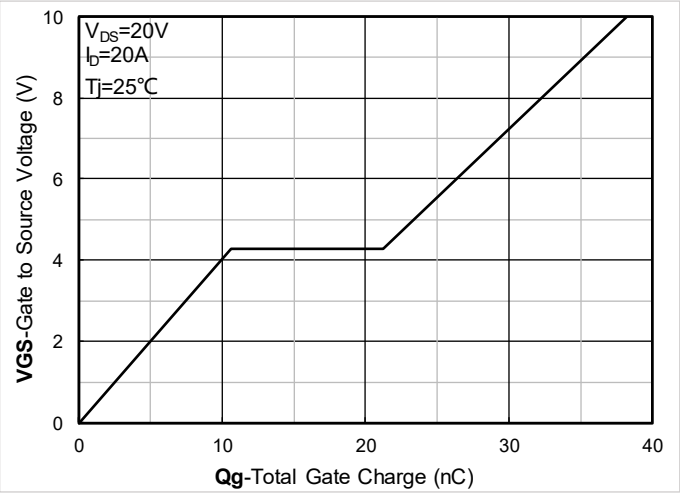



Figure 4. Gate Charge; typical values

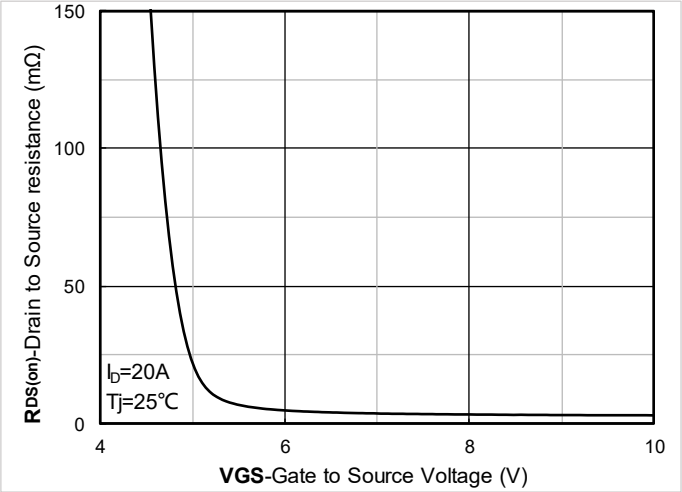



Figure 5. On-Resistance vs. Gate to Source Voltage; typical values

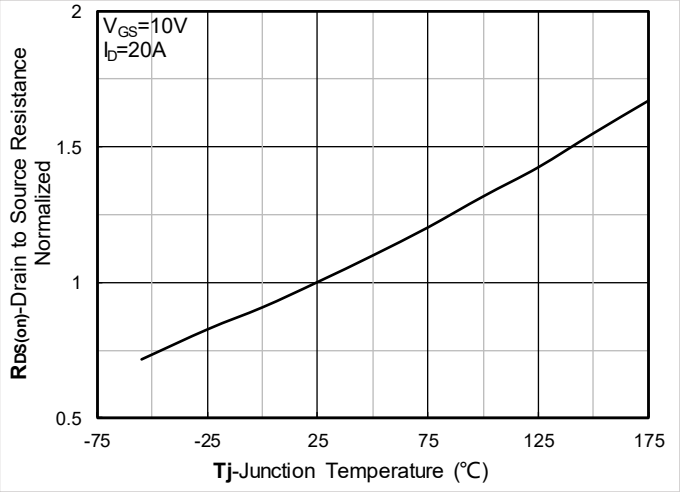



Figure 6. Normalized On-Resistance

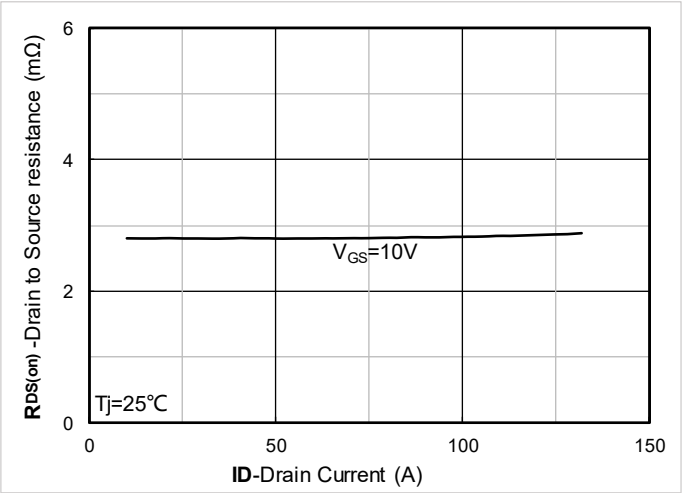



Figure 7. $R_{DS(on)}$ vs. Drain Current; typical values

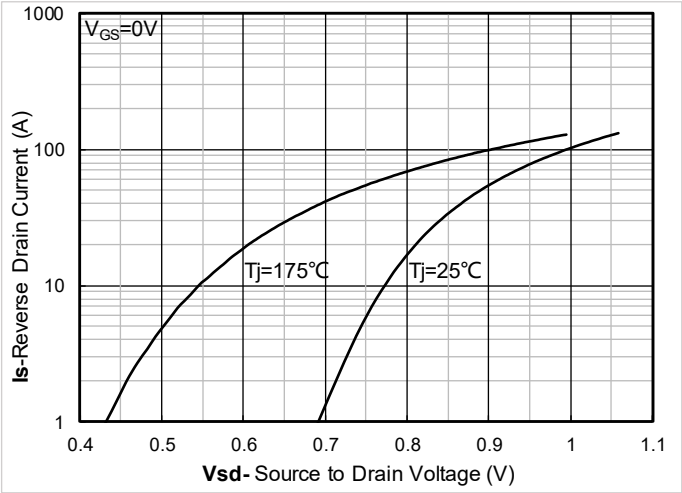



Figure 8. Forward characteristics of reverse diode; typical values

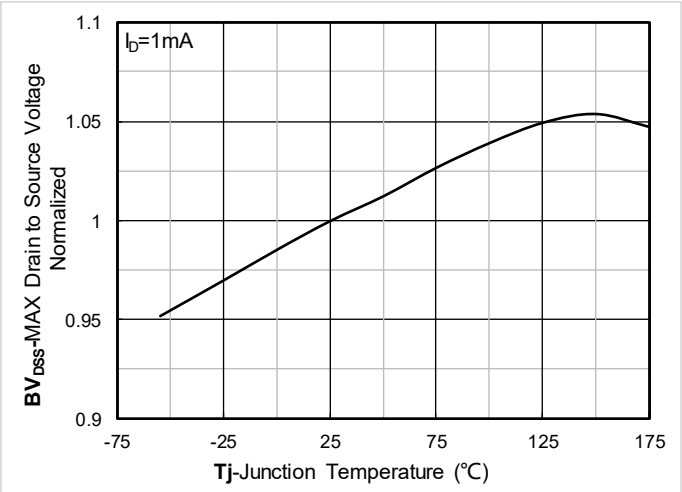



Figure 9. Normalized breakdown voltage

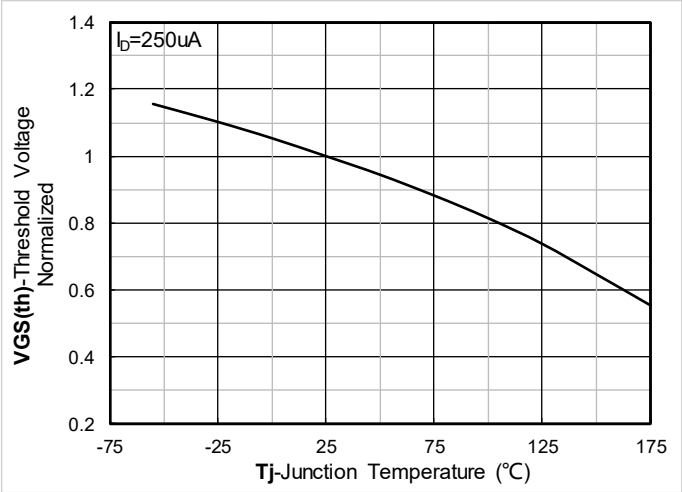



Figure 10. Normalized Threshold voltage

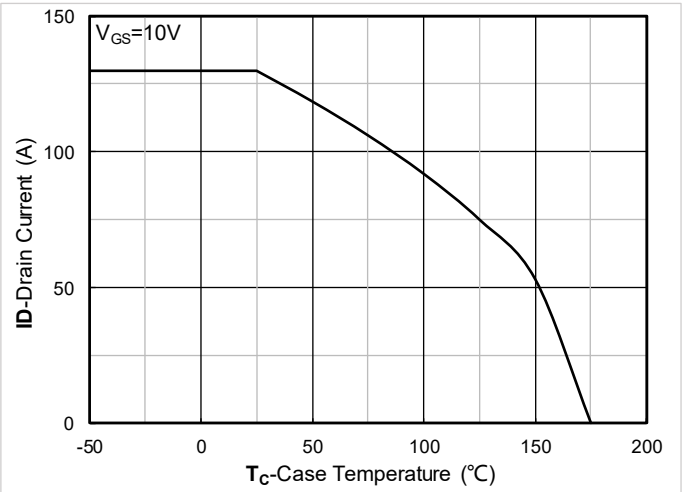



Figure 11. Current dissipation

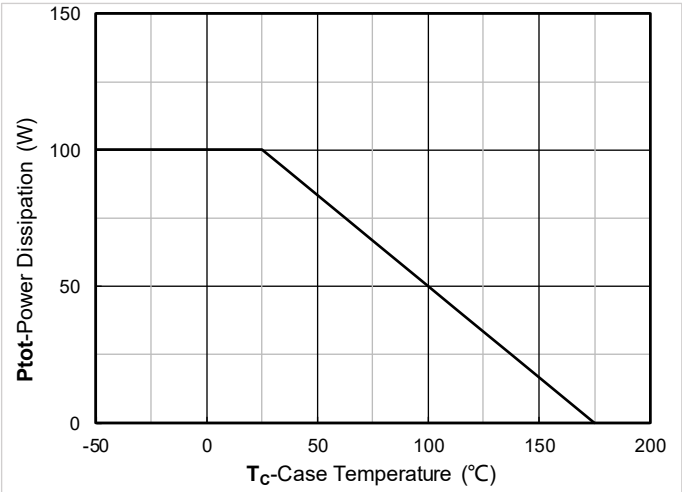



Figure 12. Power dissipation

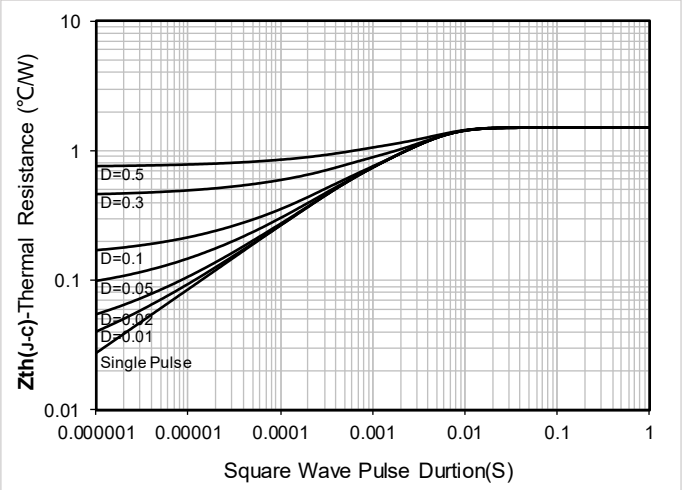



Figure 13. Maximum Transient Thermal Impedance

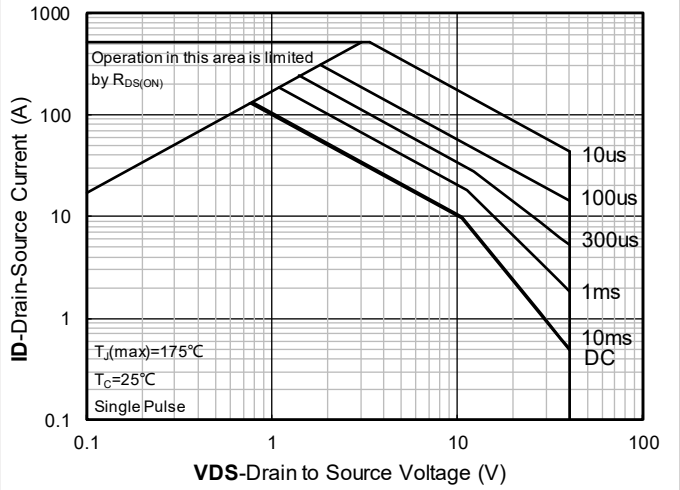



Figure 14. Safe Operation Area

## ■ Test Circuits & Waveforms

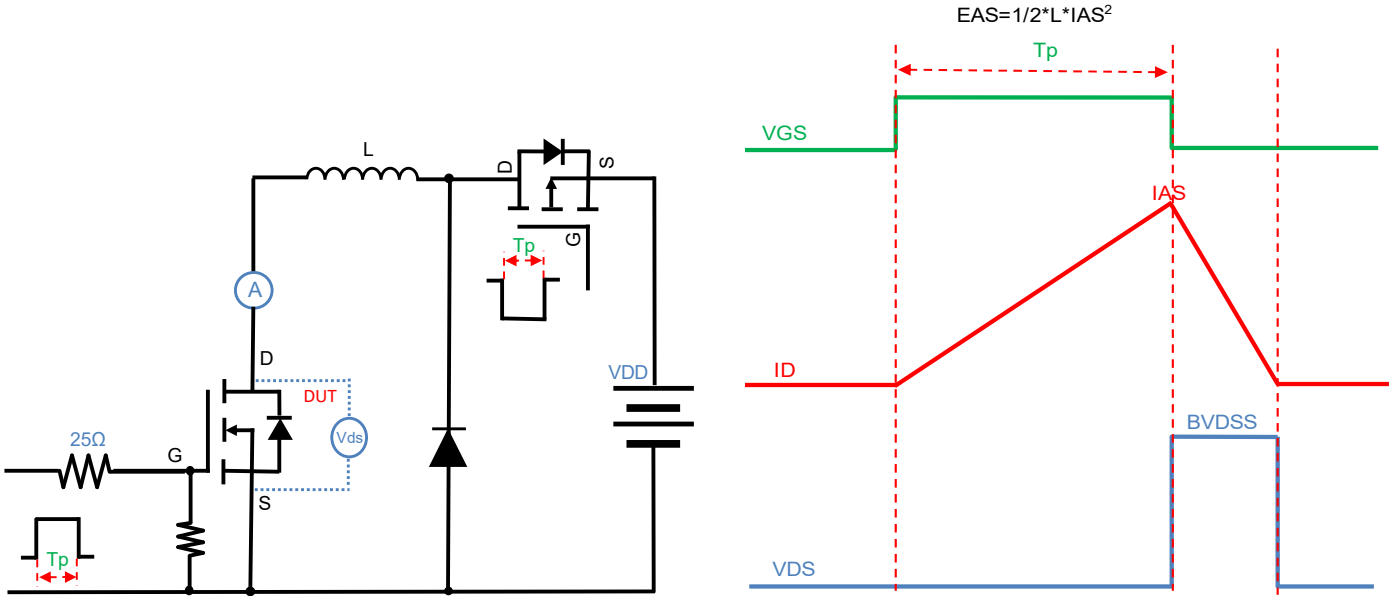



Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

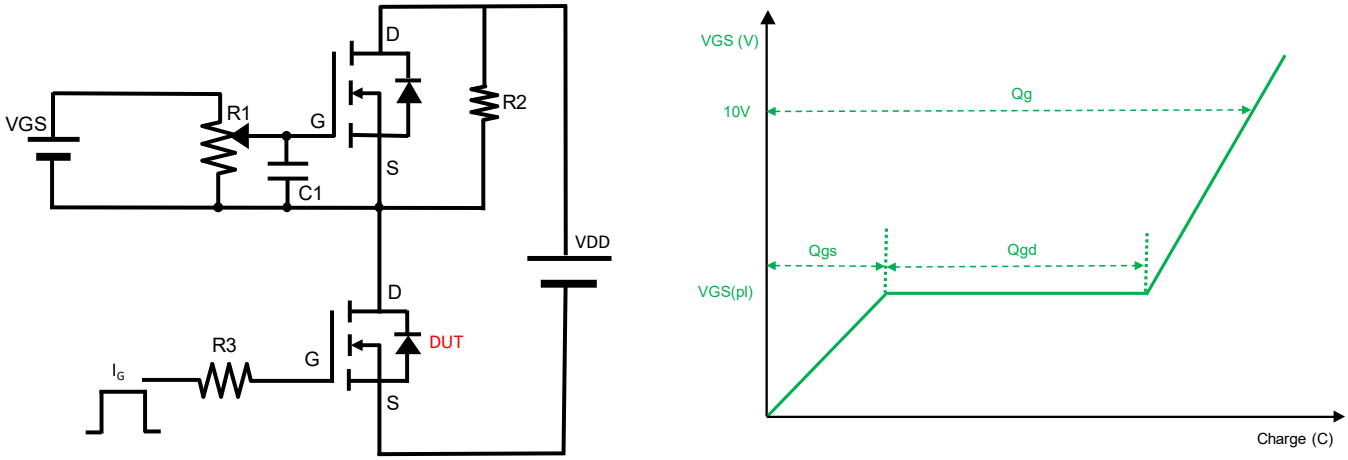



Figure B. Gate Charge Test Circuit & Waveform

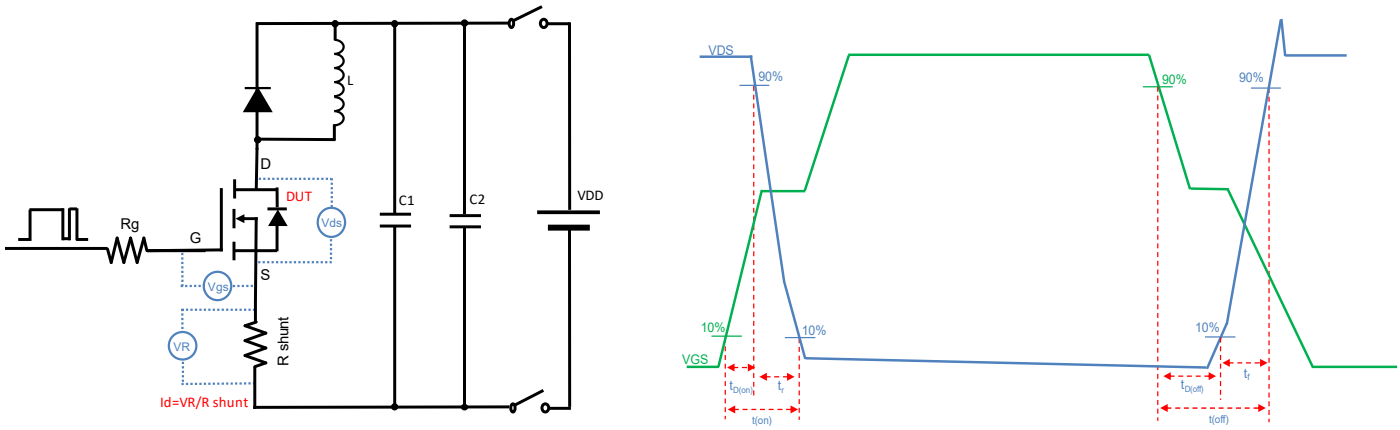



Figure C. Resistive Switching Test Circuit & Waveform

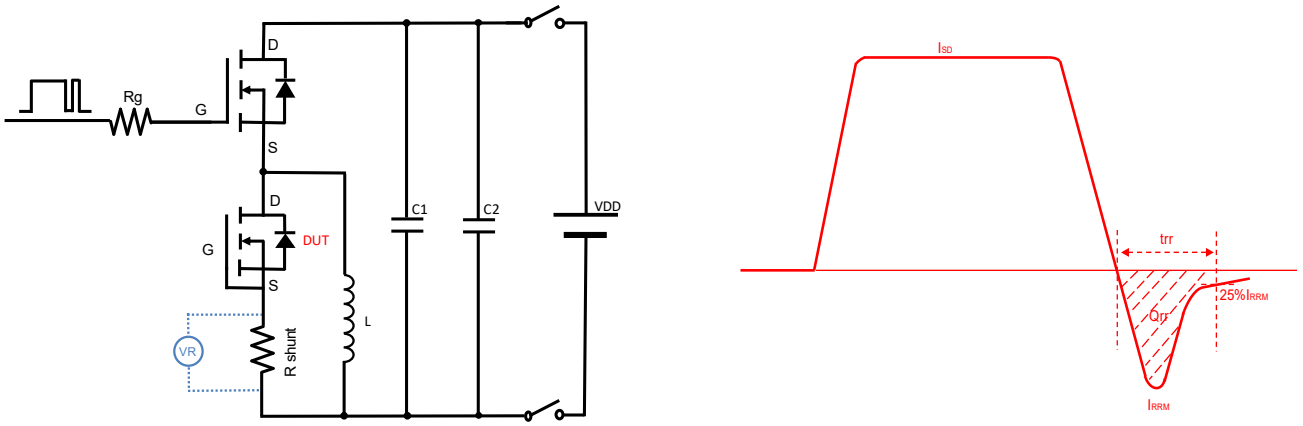
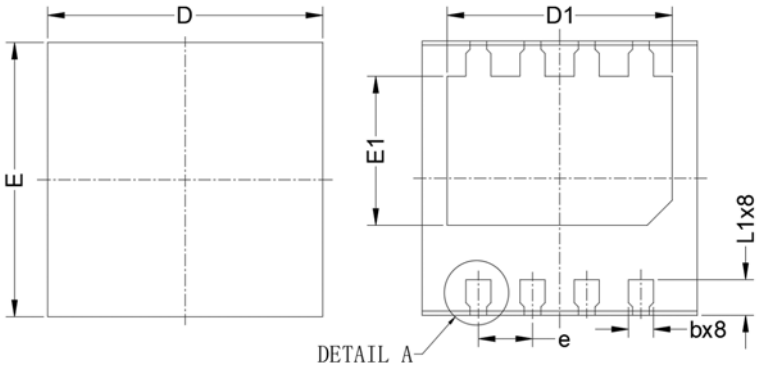



Figure D. Diode Recovery Test Circuit & Waveform

## ■ DFN3333-8L-WF Package information

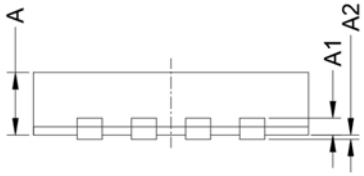



Top View
正面视图

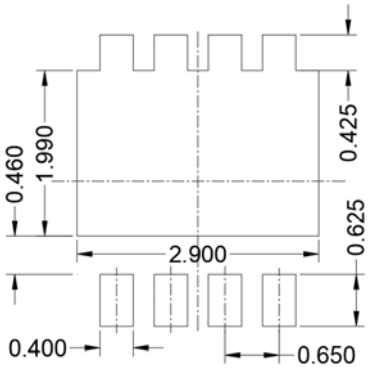
Bottom View
背面视图

| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| D | | 3.30 BSC | |
| E | | 3.30 BSC | |
| A | 0.70 | 0.75 | 0.80 |
| A1 | | 0.203 BSC | |
| A2 | | | 0.10 |
| D1 | 2.60 | 2.70 | 2.80 |
| E1 | 1.69 | 1.79 | 1.89 |
| L1 | 0.325 | 0.425 | 0.525 |
| b | 0.20 | 0.30 | 0.40 |
| e | | 0.65 BSC | |

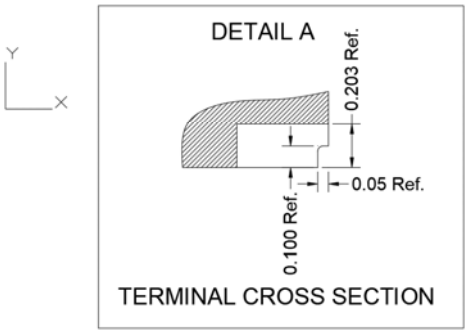
Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.10mm.
3.The pad layout is for reference purposes only.




Side View
侧面视图




Suggested Solder Pad Layout
Top View



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